APPLICATION

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TITLE: **TIME-SHIFTED VIDEO SIGNAL PROCESSING**

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Time-Shifted Video Signal Processing

Field of invention

This invention relates to time-shifted video signal processing.

Background of the Invention

A viewer of "real-time" video cannot normally perform the kinds of "trick" functions, such as pause, play, fast forward, or reverse, that are available for recorded video.

By providing a system that can play back stored material while simultaneously and continuously storing the real-time video signal, it is possible to create a user experience that is the same for both "real-time" and pre-recorded material. The play back can be delayed (time-shifted) by as much as the storage size, and as little as the system delay, referred to as "near real time". The trick functions then can be provided from the stored version.

In such a system, when real time channel changes ("channel surfing" in popular lingo) are required, the newly selected input signal must go through the whole system and be encoded, stored, and decoded before it is visible to the viewer. This causes a disconcerting time delay making a channel change operation appear sluggish. As seen in figure 1, a time-shifted system 10 may use a digitized, uncompressed video signal 12 that is derived from an incoming broadcast analog TV signal or other source. Signal 12 is encoded (compressed into, e.g., MPEG format) in an encoder 14. A host controller 20 then writes the compressed frames in a storage buffer 24 (e.g., a hard disk). For viewing, the host controller 20 reads (reading and writing occur simultaneously) the compressed video from the storage

buffer and delivers it to a video decoder 18. The video decoder produces a time-shifted decoded uncompressed output 28 that is displayed to the viewer.

The delay between the input signal and the time-shifted decoded output will vary depending on system hardware and software implementation as well as compression technique used.

The same issue holds true for compressed digital broadcast signals. As seen in figure 2, in a set-top box using a time-shifted system, the input is a transport signal 13 that carries multiplexed compressed (e.g., MPEG) digital video signals. A transport de-multiplexer 15 provides de-multiplexed compressed signals that the host controller stores and delivers as in figure 1.

Summary of the Invention

In general, in one aspect, the invention features a time-shifted video method having a real-time mode during which real-time video frames are delivered for display. In a time-shifted mode, time-shifted video frames are delivered for display. The time-shifted video frames are delayed relative to the real-time video frames. A real-time frame is paused during a transition from the real-time mode to the time-shifted mode.

Implementations of the invention may include one or more of the following features. The transition may be between the paused real-time frame and a time-shifted version of the paused real-time frame. Trick functions may be provided during the time-shifted mode. The transition mode may be triggered by a command of a viewer or an event generated by software. The real-time video frames may be derived from input uncompressed video. The real-time video frames may be provided from an input frame buffer, from

input compressed video or from a decoder that decompresses the input compressed video. The real-time mode, the time-shifted mode, and the transition may be provided by a single codec chip. The compressed video may comprise MPEG video. The information may be stored identifying the paused frame. Before the time-shifted mode occurs, the predetermined frame or the next frame after the predetermined frame may be queued up.

In general, in another aspect, the invention features apparatus that includes a port to receive an input video signal, a time-shifted processing path that stores compressed video frames based on the input video signal and delivers time-shifted stored video frames to an output, a real-time processing path that delivers real-time video to the output based on the input video signal, and control circuitry that controls transitions between the real-time video frames and the time-shifted video frames at the output.

Implementations of the invention may include one or more of the following features. The processing paths may include two decoders in a single codec. The processing paths may include buffers provided by a common memory. The apparatus may comprise a set-top box or an analog television receiver.

Among the advantages of the invention may be one or more of the following.

Incoming video signals can be viewed without going through the system pipeline, thus permitting quick channel changes. The viewer can switch seamlessly between the incoming and time-delayed video signals. Transitions to and from trick functions can be provided seamlessly. Set-top box and analog receiver implementations are possible. System bandwidth requirements are reduced and hard disc life span

increased by not having to read back from the storage media in normal "real-time" operation.

Other advantages and features will become apparent from the following description and from the claims.

Brief Description of the Drawing

Figure 1 is a block diagram of a time-shifted system that uses an uncompressed digital video input.

Figure 2 is a block diagram of a time-shifted system that uses a compressed digital video input.

Figure 3 is a block diagram of an improved time-shifted system that uses an uncompressed digital video input.

Figure 4 is a block diagram of an improved time-shifted system that uses a compressed digital video input.

Figure 5 is a flow diagram.

Figure 6 is a block diagram of a buffer configuration.

Figure 7 is a block diagram of a single-ship configuration.

Description of the Preferred Embodiments

As seen in figure 3, in an improved time-shifted system 30, incoming uncompressed video is stored in a frame buffer 29 and used to provide real-time uncompressed video 31 for display through a switch 23. In a parallel processing path, the same incoming uncompressed video 12 is used to generate a time-shifted uncompressed output 28 (in a manner similar to figure 1) that may also be delivered through switch 23.

As seen in figure 4, in another improved time-shifted system 31, in which the input is compressed digital

video 13, a second video decoder 34 is added to supplement the existing video decoder 18 of figure 2.

Decoder 34 receives the compressed transport signal directly from the transport de-multiplexer 14, decodes it, and delivers it as a real-time uncompressed output 36 with a timing T2 that is essentially the same as the timing T1 (T2 = T1) except for a small delay (D_D) associated with the decoding.

Decoder 18, on the other hand, delivers a time-shifted decoded output 28 like the one generated by decoder 18 in figure 1 with a timing T3 that is delayed relative to T1 by a delay d. Delay d can be as large as the number of frames in the storage buffer (e.g., if the viewer has chosen to play back the oldest available frames) and as small as the minimum combined delay of the storage system and the decoder 18 (e.g., if the viewer is viewing the most recently stored frames).

The systems described in figures 3 and 4 have essentially two display modes, real-time and time-shifted.

In both improved implementations, the displayed output will be switched between "time-shifted" and "near real-time" outputs as needed, using "near real-time" when viewing the live broadcast and during channel changes and "time-shifted" when doing trick modes or when viewing recorded material.

The flow of operation for switching between these modes is shown in figure 5.

If the viewer begins in real-time mode and stays in real-time mode, the system operates much as a conventional receiver, delivering the incoming uncompressed digital video signal directly from buffer 29 to the output for display through switch 23. A compressed version of the incoming video is continually generated by encoder 14 and stored in

buffer 24 but the video stored there is not used for the output during real-time display.

The display will remain in real-time mode until a trick play is requested. If the viewer commands the system to pause, the system continues to display the frame that was in the frame buffer 29 at the time the pause was invoked. The paused frame is marked with an indicator (stamp), and is encoded normally. While the real-time video is paused, encoding and storage continue to occur. The decoder decodes the stream until the marked frame is reached and then pauses on the next frame. The display is still showing the paused frame buffer 29 at this stage.

When the time-shifted decoder 18 encounters the paused frame (identified by the stamp), it effectively queues up the next frame by not advancing to process any subsequent frame in the buffer. As soon as the next-after-paused frame is queued, the host controller can switch the display output to the time-shift decoder when a single step or slow motion command is sent. The display transition from the frame buffer 29 to time-shifted material will be seamless to the viewer. Any other trick play command after pause will also cause the display output to switch, but only once the new frame or stream is queued. Doing a seamless switch in this case is not required.

Similarly, if the viewer commands a trick feature during the real-time mode, the host controller identifies the initial frame that is to be displayed to effect the trick feature, and the time-shift decoder queues up that frame. The display then switches the output video to the time-shift decoder.

When the output is switched to the time-shifted decoder, the time-shifted decoder resumes normal Decoding and the system enters the time-shift mode.

The system will remain in timeshift display mode until a channel change command, or if the viewer selects to display the live broadcast and view the program in real time. The encode and storage process continues uninterrupted during all mode changes.

As seen in figure 6, in one implementation of the system of figure 3, two frame buffers 80, 88, are used to buffer and process incoming uncompressed video and outgoing digital video frames.

The encoder frame buffer 80 includes an area 83 that stores successive incoming uncompressed digital video frames F1 ... Fn and an area 84 that stores compressed (e.g., MPEG) frames that are generated by an (MPEG) encoder 82 based on the stored video frames in area 83.

The decoder frame buffer 88 similarly has an area 86 that holds compressed frames and an area 92 that holds uncompressed video frames that are generated by time-shifted video decoder 18 from the compressed frames. The time-shifted decoded output 28 is displayed from the video frame area 92. The real-time output 31 is displayed from area 83 of buffer 80.

The following paragraphs describe an internal implementation of a single CODEC solution for real-Time viewing and seamless switching to time-shifted material. The CODEC in this implementation is capable of sharing its memory between the encode and decode operations.

We describe this implementation with reference to figure 6 and also with respect to figure 5. For encoding, the incoming digital video frames 78 are buffered into the encoder frame buffer area of the memory 80 before they are encoded. The number of frames buffered will depend on the compression method used. For MPEG2 IBBP, for example, at least enough frames must be stored to encode the next P

frame. Each frame is encoded by encoder 82 in the order prescribed by the compression algorithm used, then stored as a compressed frame 84 in the frame buffer ready for transfer to the host.

In decoding, the process is reversed. Compressed video frames are first transferred into a decoder compressed frame buffer area 88 of the memory. The frames are decoded by decoder 18, and the uncompressed frames are written to the decoder's video data buffer area of the memory 92 for display.

In typical operation, when the user is viewing in real-time, the display output of switch 23 is set to the real-time output 31, which is continually displaying the memory buffer containing the latest fully captured frame of video. The decoder 18 in this mode can be idle since nothing is displayed from its frame buffer 88. This mode is indicated in block 201 of figure 5.When a seamless switch from real-time to time-shifted display is needed (e.g., when a user selects pause 203, then step),the display output 31 of the codec chip will be paused by reserving this memory area and keeping the display window set to the last captured frame in the encoder frame buffer 205. Because the decoder output is not being viewed during this mode, it is possible to reclaim some of the decoder frame buffer 88 for use by the encoder. This is required since one frame area is locked in the pause mode but the encoder 82 still must continue encoding and needs all of its normally prescribed memory space.

To achieve a seamless transition to the time-shifted output 28 once the real-time frame is paused, the same encoded frame must also be queued and ready to display at the output of the decoder. When the pause function is invoked, the paused frame is encoded, marked, and stored

normally 207. The resulting video stream is then read back to the decoder, decoded, but not written to the display buffer 83 (now used by the encoder). When the marked frame is reached, the decoded result is written to the decoder frame buffer 88, ready for display 209. The output display is switched 211 as soon as the frame has been decoded and ready for display, and the locked memory area that was being used for the freeze frame is released back to the decoder. The display remains in time-shifted view 213 as long as it is not required to switch back to live (e.g., channel change 215). An alternative way to implement the switch to time-shift is to queue up the frame following the marked frame, and only switch once the next command is issued.

In the case of a system, like the one in figure 4, in which the input is a compressed digital signal, a second decoder is required to provide the "real-time" view and the flow chart of figure 5 would be generally the same. However, while the minimum delay in the system of figure 3 of the time-shifted signal would be $D_E + D_S + D_D$, the minimum delay in the system of figure 4 would be only $D_S + D_D$. Also, in figure 3, the real-time output has a delay of one frame compared to the input (caused by the frame buffer) while in figure 4, the delay is D_D frames

An efficient way to implement the system of figure 4 is to use a single codec chip of a kind that has the capability to decode (decompress) two incoming digital video signals simultaneously to perform the functions of both decoders 18 and 34.

As seen in figure 7, such a single chip codec 108, when combined with a common memory 106, may be used to implement a time-shifted system 100 that can handle both incoming compressed and incoming uncompressed video signals 104, 102. Memory 106 serves the functions of both of the

buffers 80, 88 of figure 5. The resulting digital video output 111 is controlled by the host controller to be either real-time or time-shifted as needed.

Other implementations are within the scope of the following claims. For example, the paused frame may be marked by inserting the mark in the bitstream or the frame header, or by indexing in the system software. For a compressed digital video signal system as described in Figure 4, no marking is possible since the stream is not being manipulated, however, methods such as reading back the presentation time stamp from the decoder 34 can be used to queue up decoder 18 to the frame being paused.

The invention can be implemented in a set-top box which is capable of handling either a compressed video input, an uncompressed video input, or both.

What is claimed is: